REMARKS

The July 11, 2008 Final Office Action was based upon pending Claims 2-7, 9-12, 14-16, 23-29, 31-35, 37 and 39-54. This response amends Claims 2, 10, 23, 31, 37, and 44. Thus, after entry of this response, Claims 2-7, 9-12, 14-16, 23-29, 31-35, 37 and 39-54 are pending and presented for further consideration.

ISSUES RAISED IN THE OFFICE ACTION

The Office Action rejected Claims 2-7, 9-12, 14-16, 23-29, 31, 33-35, 37 and 39-54 under 35 U.S.C. §103(a) as being unpatentable over Solari, U.S. Patent No. 5,333,276, in view of Amini, et al., U.S. Patent No. 5,644,729, and further in view of Carlson, et al., U.S. Patent No. 5,692,200.

The Office Action also rejected Claims 32 and 43 under 35 U.S.C. §103(a) as being unpatentable over Solari, Amini, et al, and Carlson, et al., as applied to Claims 31 and 23 , and further in view of Rabe, et al., U.S. Patent No. 5,664,122.

REJECTION OF CLAIMS 2-7, 9-12, 14-16, 23-29, 31, 33-35, 37 AND 39-54 UNDER 35 U.S.C. §103(a)

The Office Action rejected Claims 2-7, 9-12, 14-16, 23-29, 31, 33-35, 37 and 39-54 under 35 U.S.C. §103(a) as being unpatentable over Solari, in view of Amini, and further in view of Carlson.

Claim 2

Neither Solari, Amini, nor Carlson, appear to teach the concept of bi-directional data transfers between a processor and a component wherein a bi-directional data buffer is matched with an address buffer such that the bi-directional data buffer is configured to hold the data read from the component.

As stated by the Examiner, Solari does not teach the bi-directional transfer of data. Furthermore, neither Amini, nor Carlson teach, for example, the concept of allocating a bi-directional data buffer that is matched with an address buffer.

In this example, when the processor issues a read request, the matched bi-directional data buffer is configured to hold a data value requested by the processor

from the component. In addition, when the processor issues a write request, the bi-directional data buffer holds that data being written to the component.

None of the cited references appear to teach such concepts. Furthermore, it would not have been obvious to add this concept in light of the teachings of the cited references. For example, neither Amini nor Carlson, allocate a bi-directional data buffer to hold a data value requested by a processor wherein the bi-directional data buffer is matched with the address buffer associated with the request.

In particular, neither Solari, Amini, nor Carlson teach a method for providing data transfers between a processor and a component, the method comprising:

routing requests originating from a component to a processor through a target controller and handling requests originating from the processor to the component by;

buffering a first address with a first address buffer in response to a read request originating from the processor to the component, and associating a first bi-directional data buffer with the first address wherein the first bi-directional data buffer is configured to hold a first data value requested by the processor from the component;

buffering a second address with a second address buffer in response to a write request originating from the processor to the component, and associating a second bi-directional data buffer with the second address wherein the second bi-directional data buffer is configured to hold a second data value written by the processor to the component, the first and second address buffers being in communication with the processor and the component, wherein the processor operates at a different speed than the component;

buffering the first data value requested by the processor with the first bi-directional data buffer when the data is obtained from the component and buffering the second data value written by the processor with the second bi-directional data buffer, the first and second bi-directional data buffers being in communication with the processor and the component, wherein the first and second address buffers are separate from the first and second data buffers;

monitoring the first and second address buffers and the first and second data buffers to determine when the first address and data buffers have obtained the first data value requested by the processor and the second address and data buffers have written the second data value to the component ;

controlling the first address buffer and the first bi-directional data buffer as a matched pair such that the first address held in the first address buffer corresponds to the first data value requested by the processor from the component;

controlling the second address buffer and the second bi-directional data buffer as a matched pair such that the second address held in the second address buffer corresponds to the second data value written by the processor to the component ;

reading status information from the first address buffer to determine a priority status of the first data value;

reading status information from the second address buffer to determine the priority status of the second data value; and

controlling the order of bi-directional data flow through the first and second bi-directional data buffers such that data flows between the processor and the component while the processor is processing other instructions and, wherein controlling the order of the bi-directional data flow through the first and second bi-directional data buffers is variable and based on the priority status of the first and second data values.

Given the significant differences between amended Claim 1 and the cited references, Applicant respectfully requests allowance of Claim 1.

Claims 3-7, 9 and 50

Claims 3-7, 9, and 50 which depend from Claim 2, are believed to be patentable for the same reasons articulated above with respect to Claim 2, and because of the additional features recited therein.

Claim 10

Neither Solari, Amini, nor Carlson teach a method for controlling data transfers between a processor and a component, the method comprising:

routing requests from a component for data from a processor through a target controller and routing requests from the processor for data from the component;

buffering with a plurality of address buffers, the requests from the component to the processor;

buffering with a plurality of address buffers, the requests from the processor to the component, wherein the processor operates at a different speed than the component;

associating a plurality of bi-directional data buffers with the address buffers such that at least one bi-directional data buffer is matched with at least one address buffer for each request, and wherein the bi-directional data buffers are configured to hold data to be obtained from either the component or the processor;

storing status information in each of the plurality of address buffers, the status information determining the priority status of data transfers associated with the address requests;

monitoring the plurality of address buffers and the first to determine when address buffers have completed a task and are available for a further task;

bi-directionally buffering with a plurality of bi-directional data buffers data transfers between the processor and the component, wherein said data transfers can be performed out of a previously defined order based on the priority status of each of the data transfers and such that data transfers can be performed while the processor is processing other instructions; and

controlling said buffering address requests and said bi-directionally buffering through said plurality of bi-directional data buffers such that each of the buffered data transfers relates to an address held in one of the plurality of address buffers.

Given the significant differences between amended Claim 10 and the cited references, Applicant respectfully requests allowance of Claim 10.

Claims 11, 12, 14-16, and 51

Claims 11, 12, 14-16, and 51 which depend from Claim 10, are believed to be patentable for the same reasons articulated above with respect to Claim 10, and because of the additional features recited therein.

Claim 23

Neither Solari, Amini, nor Carlson teach a method for transferring addresses and data through a bi-directional buffer, the method comprising:

routing requests of a first component originating from a second component through a target controller and handling requests originating from the first component by;

storing a first address in a first buffer in communication with the first component and the second component, the first buffer comprising status bits and wherein the first address is associated with a first read request from the first component to the second component;

storing first data associated with the first read request in a second bi-directional buffer matched with said first buffer so that the first address stored in the first buffer is related to the first data stored in the second bi-directional buffer;

storing a second address in a third buffer in communication with the first component and the second component, the third buffer comprising status bits and wherein the second address is associated with a second read request from the second component to the first component;

storing second data associated with the second read request in a fourth bi-directional buffer matched with said third buffer so that the second address stored in the third buffer is related to the second data stored in the fourth bi-directional buffer;

monitoring the first and second address buffers and the first and second data buffers to determine when the first address and data buffers and the

second address and data buffers have completed a task and are available for a further task;

reading the status bits of the first buffer to determine a first priority value of the first data;

reading the status bits of the third buffer to determine a second priority value of the second data; and

controlling the order of bi-directional data flow of the first data and the second data through said second and fourth bi-directional buffers in a variable manner based at least in part on said first and second priority values and controlling the bi-directional data flow such that data flows with processing by the second component of other instructions.

Given the significant differences between amended Claim 23 and the cited references, Applicant respectfully requests allowance of Claim 23.

Claim 24-29 and 52

Claims 24-29 and 52, which depend from Claim 23, are believed to be patentable for the same reasons articulated above with respect to Claim 23, and because of the additional features recited therein.

Claim 31

Neither Solari, Amini, nor Carlson, either alone or in combination, teaches a method for transferring data between a processor and a component utilizing a plurality of address buffers and a plurality of data buffers, the method comprising:

receiving a first request that originates from the processor, receiving the first request including an associated first address from the processor;

determining whether at least one of a plurality of address buffers and an associated bi-directional data buffer are available, wherein the associated bi-directional data buffer is configured to buffer the data identified by the first address from the processor;

storing the first address in the at least one address buffer;

storing status information indicative of a priority of the first request in the at least one address buffer;

buffering data identified by the first address with the bi-directional data buffer, wherein the data is obtained from a component and is provided to the processor; and

ordering, based on the priority of the first request, the transmission of the data from the bi-directional data buffer to the processor and such that data flows bi-directionally with processing by the processor of other instructions; and

receiving a second request that originates from the component, the second request including a second address;

determining whether at least one of the plurality of address buffers and associated bi-directional data buffers are available, wherein the associated bi-directional data buffer is configured to buffer the data identified by the second address from the component;

storing the second address in the at least one address buffer; and

buffering data identified by the second address with the bi-directional data buffer, wherein the data is obtained from the processor and is provided to the component.

Given the significant differences between amended Claim 31 and the cited references, Applicant respectfully requests allowance of Claim 31.

Claim 33-35 and 53

Claims 33-35 and 53, which depend from Claim 31, are believed to be patentable for the same reasons articulated above with respect to Claim 31, and because of the additional features recited therein.

Claim 37

Neither Solari, Amini, nor Carlson, either alone or in combination, teaches an apparatus for controlling data transfers between a processor and a component, the apparatus comprising:

means for buffering at least a first address associated with a first request from a processor to a component and buffering at least a second address associated with a second request from a component to a processor;

means for bi-directionally buffering data transfers between the processor and the component, that are associated with the first and second addresses;

means for storing status information indicative of a priority status of the buffered data transfers;

means for controlling the means for buffering and the means for bi-directionally buffering so that each of the buffered data transfers relates to the first and second addresses held in the means for buffering, wherein the means for controlling further coordinates an order of said data transfers based at least on the priority status of each buffered data transfer and such that data flows bi-directionally with processing by the processor of other instructions; and

means for routing the data transfers from the processor to the component and routing the data transfers from the component to the processor.

Given the significant differences between amended Claim 37 and the cited references, Applicant respectfully requests allowance of Claim 37.

Claims 39-43

Claims 39-43, which depend from Claim 39, are believed to be patentable for the same reasons articulated above with respect to Claim 39, and because of the additional features recited therein.

Claim 44

Neither Solari, Amini, nor Carlson, either alone or in combination, teaches a buffer allocation system for managing data flow between components of a computer, the system comprising:

an address buffer module configured to handle address requests between a first component and a second component for requests originating from the first component and the second component, the address buffer module comprising:

a plurality of address buffers each in communication with the first and second components, each address buffer comprising status information indicative of a priority status;

an input address arbiter configured to direct the address requests from the first and second components to the plurality of address buffers; and

an output address arbiter configured to send the address requests from the first component to the second component from the plurality of address buffers and to send the address requests from the second component to the first component from the plurality of address buffers; and

a data buffer module configured to control an order of bi-directional flow of data therethrough between the first and second components based on the priority status of the data and such that data flows bi-directionally with processing by the first component of other instructions, the data buffer module comprising:

a plurality of bi-directional data buffers each in communication with the first and second components, wherein one or more of the bi-directional data buffers is paired with one or more of the address buffers such that the bi-directional data buffers are configured to buffer the data to be obtained from the addresses buffered in the paired address buffers;

an input data arbiter configured to direct data to the plurality of bi-directional data buffers; and

an output data arbiter configured to direct data output from the plurality of bi-directional data buffers; and

a target controller configured to route requests between the first and second components.

Given the significant differences between amended Claim 44 and the cited references, Applicant respectfully requests allowance of Claim 44.

Claims 45-49 and 54

Claims 45-49 and 54, which depend from Claim 44, are believed to be patentable for the same reasons articulated above with respect to Claim 4, and because of the additional features recited therein.

REJECTION OF CLAIMS 32 and 43 UNDER 35 U.S.C. §103(a)

The Office Action rejected Claims 32 and 43 under 35 U.S.C. §103(a) as being unpatentable over Solari, Amini, et al, and Carlson, et al., as applied to Claims 31 and 23 , and further in view of Rabe, et al., U.S. Patent No. 5,664,122.

Claim 32

Claim 32, which depends from Claim 31, is believed to be patentable for the same reasons articulated above with respect to Claim 31, and because of the additional features recited therein.

Claim 43

Claim 43, which depends from Claim 23, is believed to be patentable for the same reasons articulated above with respect to Claim 23, and because of the additional features recited therein.

CO-PENDING APPLICATIONS OF ASSIGNEE

The Applicant wishes to draw the Examiner's attention to the following co-pending applications of the present application's assignee.

Appl. No.	Filing Date	Attorney Docket No.	Title
08/896,938, now U.S. Patent No. 6,073,190	07/18/97	MTIPAT.002A	SYSTEM FOR DYNAMIC BUFFER ALLOCATION COMPRISING CONTROL LOGIC FOR CONTROLLING A FIRST ADDRESS BUFFER AND A FIRST DATA BUFFER AS A MATCHED PAIR
09/589,043, now U.S. Patent No. 6,601,118	06/06/00	MTIPAT.002C1	DYNAMIC BUFFER ALLOCATION FOR A COMPUTER SYSTEM

Applicant notes that cited references, office actions, responses and notices of allowance currently exist or will exist for the above-referenced matters. Applicant also understands that the Examiner has access to sophisticated online Patent Office computing systems that provide ready access to, for example, specification and drawing publications, pending claims and complete file histories, including, for example, cited art, office actions, responses, and notices of allowance.

Applicant respectfully requests that the Examiner continue to review these file histories for current information about these matters. However, if the Examiner cannot readily access these file histories, the Applicant would be pleased to provide any portion of any of the file histories at any time upon specific Examiner request.

RESCISSION OF ANY PRIOR DISCLAIMERS AND REQUEST TO REVISIT ART

The claims of the present application are different and possibly broader in scope than any pending claims in any related application or issued claims in any related patent. In particular, in one or more parent applications, including (1) U.S. Patent Application No. 08/896,938, filed June 18, 1997, now U.S. Patent No. 6,073,190, issued June 6, 2000; and (2) U.S. Patent Application No. 09/589,043, filed June 6, 2000, now U.S. Patent No. 6,601,118, issued July 29, 2003.

To the extent that any amendments or characterizations of the scope of any claim or referenced art could be construed as a disclaimer of any subject matter supported by the present disclosure, Applicant hereby rescinds and retracts such disclaimer. Accordingly, the above-listed references, or other listed or referenced art may need to be re-visited.

In addition, reviewers of this or any parent, child or related prosecution history shall not reasonably infer that Applicant has made any disclaimers or disavowals of any subject matter supported by the present application.

CONCLUSION

In view of the foregoing, the present application is believed to be in condition for allowance, and such allowance is respectfully requested.

If further issues remain to be resolved, the Examiner is cordially invited to contact the undersigned such that any remaining issues may be promptly resolved.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

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Dated: 9-9-08

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